REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 1-30 are pending. Claims 1, 6, 11, 12, 21, 25, and 28 are currently amended. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

The specification stands objected to because the title of the invention is not descriptive.

Claims 1-11, 15, and 30 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as his invention. Although the Office Action states that claims 1-11, 15, and 30 are rejected under 35 U.S.C. § 112, second paragraph. Applicant notes that the Office Action merely presents arguments for rejecting claims 1, 3, 5, 6, 11, 15, 20, 21, 23, 25, and 28. Thus, for purposes of this response, Applicant has responded to the actual arguments presented for claims 1, 3, 5, 6, 11, 15, 20, 21, 23, 25, and 28.

Claims 1-7, 9-11, 25, 26, and 29 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,007,211 to White et al. (hereinafter "White")

Claims 8, 12-24, 27, and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over White in view of U.S. Patent No. 6,779,144 to Hayashi et al. (hereinafter "Hayashi").

Response to Objections

The specification stands objected to because the title of the invention is not descriptive. In particular, the Office Action states that a new title is required that is clearly indicative of the invention to which the claims are directed. Although Applicant believes the original title of the application is descriptive, Applicant respectfully submits

that the title has been amended to "A method and apparatus for a command based BIST for testing memories," as suggested by the Examiner. Applicant appreciates the Examiner's recommendation and respectfully requests that the objection to the specification be withdrawn.

Response to Rejections under 35 U.S.C. § 112, second paragraph

The Office Action rejected claims 1, 3, 5, 6, 11, 15, 20, 21, 23, 25, and 28 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully requests withdrawal of these rejections for the following reasons.

Claims 1, 3, 5, 20, and 23 were rejected for reciting "representations of a march element" because the claim purportedly fails to define the march element with respect to the command, and because it is purportedly unclear if the "March" element and data is part of the command. In regard to the reference to "march element" in claim 1, Applicant respectfully submits that the claim language is definite because the term "march element" is known in the art. Nevertheless, Applicant has amended the claim to clarify the relationship of the march element and data as they relate to the command. In particular, claim 1 has been amended to recite "wherein the processor loads a command via the serial bus, wherein the command comprises representations of a march element and data." Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. § 112, second paragraph, be withdrawn. Similarly, Applicant respectfully requests that the rejections of claims 3, 5, 20, and 23 under 35 U.S.C. § 112, second paragraph, be withdrawn because the meaning of these claims is clear and definite in light of the known meaning of "march element" and the language of the claims.

Claims 6, 15, and 21 were also rejected for similar reasons to claims 1, 3, 5, 20, and 23. Accordingly, Applicant respectfully requests that the rejections of claims 6, 15, and 21 under 35 U.S.C. § 112, second paragraph, be withdrawn for similar reasons to those outlined above. Also, Applicant notes that the rejection of claim 15 under 35 U.S.C. § 112, second paragraph, is inappropriate because claim 15 does not include the indicated language. It appears that the Examiner intended to designate claim 16 as

including the indicated language, in which case Applicant respectfully submits that the language of claim 16 is also clear and definite for the reasons outlined above.

Claim 6 was also rejected for reciting "may be" because it is unclear if the limitations following the phrase "may be" are part of the claimed invention. Applicant respectfully submits claim 6 has been amended to remove the indicated language. Accordingly, Applicant requests that the rejection of claim 6 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claim 11 was rejected for reciting "that string" because there is insufficient antecedent basis for this limitation. Applicant respectfully submits that claim 11 has been amended to refer to "the series of bits" according to accepted antecedent basis conventions. Accordingly, Applicant requests that the rejection of claim 11 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claims 25 and 28 were rejected for reciting "communicating the compressed information in a serial manner to logic bounding the memory" because the phrase "in a serial manner" purportedly fails to positively identify the communication of the compressed information. Applicant respectfully submits claims 25 and 28 have been amended to clarify the language of the claims. Accordingly, Applicant requests that the rejection of claims 25 and 28 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Response to Rejections under 35 U.S.C. § 102(e)

The Office Action rejected claims 1-7, 9-11, 25, 26, and 29 under 35 U.S.C. § 102(e) as being anticipated by White. Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

CLAIMS 1-11

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by White. Applicant respectfully submits that claim 1 is patentable over the cited reference because White does not disclose all of the limitations of the claim. Claim 1, as amended, recites:

> An apparatus, comprising:
>
> two or more memories, wherein each memory has an intelligence wrapper bounding that memory;
>
> a processor to initiate a Built in Self Test for the memories; and

a serial bus coupled between the processor and each memory; wherein the processor loads a command containing representations of a march element and data via the serial bus.
(Emphasis added).

In support of the rejection, the Office Action states, in part:

> . . . through **a serial bus** situated between a central controller 30 and the remote processor interface (RPI) 50.
> Office Action, September 6, 2006, p.4 (emphasis added).

Applicant respectfully submits White fails to disclose all of the limitations of the claim. In particular, White does not disclose a serial bus coupled between the processor and each memory. White merely discloses a status bus 36 between the central controller 30 and each built-in self-tester 22. White, Fig. 1. White describes the status bus as a parallel bus because it has one line for each bit of the status indicator. White, col. 3, lines 23-26. Although White also states that the status bus may have any other suitable number of lines to transport the status indicator, this also does not teach a serial bus. Rather, this statement merely teaches that the parallel status bus may have few lines or many lines. However, White does not indicate that multiple bits of the status indicator may use the same line in a serial manner. Therefore, White does not disclose a serial bus between the central controller and each built-in self-tester.

In contrast, claim 1 recites "a serial bus coupled between the processor and each memory." For the reasons stated above, White fails to disclose all of the limitations of claim 1. In particular, White does not disclose a serial bus coupled between the processor and each memory. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 1 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 102(e) be withdrawn.

Given that claims 2-11 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 2-11 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 2-7 and 9-11 under 35 U.S.C. § 102(e) and the rejection of claim 8 under 35 U.S.C. § 103(a) be withdrawn.

CLAIMS 25-30

Claim 25 stands rejected under 35 U.S.C. § 102(e) as being anticipated by White. Applicant respectfully submits that claim 25 is patentable over the cited reference because White does not disclose all of the limitations of the claim. Claim 25, as amended, recites:

> A method, comprising:
>
> compressing information used in a self test of a memory embedded on a chip; and
>
> **communicating the compressed information via a serial bus to logic bounding the memory**.
>
> (Emphasis added).

In support of the rejection, the Office Action states, in part:

> **Compressing information by serially loading a pattern** using a Built In Self Test 22 for the memories (20a...20n) through **a serial bus situated between a central controller 30 and the remote processor interface (RPI) 50** . . .
>
> Office Action, September 6, 2006, pp 5-6 (emphasis added).

Applicant respectfully submits the Office Action fails to establish a *prima facie* rejection because White does not disclose all of the limitations of the claim. The Office Action also fails to establish a *prima facie* rejection because the Office Action's assertion regarding the bus between the controller and the RPI is inapposite.

To clarify what White actually discloses, White indicates that the built-in self-tester supplies a "series of patterns" to memory. White, col. 4, lines 63-67. Despite the Office Action's assertion, this is different from "serially loading a pattern." The phrase "series of patterns" used in White merely indicates that multiple patterns are supplied to memory. For example, a first pattern is supplied, and then a second pattern is supplied, and so on. This is the proper meaning of the phrase "series of patterns." However, the Office Action has mischaracterized this phrase into something that it is not. In fact, White does not disclose serially loading a pattern because White does not disclose using a serial bus. As discussed above, the status bus between the central controller and the built-in self-testers is a parallel bus.

Moreover, the Office Action fails to even assert that the status bus between the central controller and the built-in self-testers might possibly be a serial bus. The Office Action merely asserts (without basis) that another line in the system of Figure 1 is a serial bus. However, even if the line between the central controller and the RPI were a serial

bus, this line nevertheless would not be used to communicate information to the built-in self-testers because it is not even coupled to the built-in self-testers. Thus, the Office Action's assertions are inapposite because they do not indicate a line capable of facilitating the operation described in the claim. Therefore, White does not disclose communicating data from the controller to the built-in self-testers over a serial bus.

Additionally, White does not disclose compressed information. White merely discloses sending the status indicator from the controller to the built-in self-testers over the status bus. White, col. 3, lines 23-26. Similarly, White merely discloses sending monitoring information between the controller and the RPI. White, col. 4, lines 32-36. Neither of these data transmissions is disclosed to be compressed information. Therefore, White does not disclose compressed information.

In contrast, claim 25 recites "communicating the compressed information via a serial bus to logic bounding the memory." For the reasons stated above, White fails to disclose all of the limitations of claim 25. In particular, White does not disclose communicating the compressed information via a serial bus to logic bounding the memory. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 25 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 25 under 35 U.S.C. § 102(e) be withdrawn.

Independent claim 28 also includes a limitation that is similar to the limitation of claim 25. Given that the claims include similar limitations, even though each claim should be interpreted according to the language of the claim itself and not other claims, claim 28 should be patentable over the cited reference for at least the same reasons as claim 25. Claim 28 also may be patentable over the cited reference for additional reasons. Accordingly, Applicant requests that the rejection of claim 28 under 35 U.S.C. § 102(e) be withdrawn.

Given that claims 26, 27, 29 and 30 depend from independent claims 25 and 28, which are patentable over the cited reference, Applicant respectfully submits that dependent claims 26, 27, 29, and 30 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 26 and 29 under 35 U.S.C. § 102(e) and the rejection of claims 27 and 30 under 35 U.S.C. § 103(a) be withdrawn.

Response to Rejections under 35 U.S.C. § 103(a)

The Office Action rejected claims 8, 12-24, 27, and 30 under 35 U.S.C. § 103(a) as being unpatentable over White in view of Hayashi. Applicant respectfully requests withdrawal of these rejections because the combination of cited references fails to teach or suggest all of the limitations of the claims.

CLAIMS 12-24

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over White in view of Hayashi. Applicant respectfully submits that claim 12 is patentable over the combination of cited references because the combination does not teach or suggest all of the limitations of the claim. Claim 12, as amended, recites:

> An apparatus, comprising:
>
> two or more memories, each memory has an intelligence wrapper bounding that memory; and
>
> a processor to initiate a Built In Self Test for the memories, wherein a first intelligence wrapper contains **control logic to decode a compressed command from the processor** and to execute a set of test vectors on a bounded memory, wherein the processor sends a compressed command based self test to the first intelligence wrapper at a first speed and the control logic executes the operations associated with that command at a second speed asynchronous with the first speed.

(Emphasis added).

Applicant respectfully submits the combination of White and Hayashi does not disclose all of the limitations of the claim. In particular, the combination of White and Hayashi does not disclose control logic to decode a compressed command from the processor.

In regard to White, Applicant explained above that White does not disclose compressed information. White merely discloses sending the status indicator from the controller to the built-in self-testers over the status bus. White, col. 3, lines 23-26. Similarly, White merely discloses sending monitoring information between the controller and the RPI. White, col. 4, lines 32-36. Neither of these data transmissions is disclosed to be compressed information. Therefore, White does not disclose compressed information.

Hayashi also fails to disclose control logic to decode compressed information from the processor. Although Hayashi contains a reference to compressed information at col. 12, lines 41-45, this reference is directed to compressed data held by a flip-flop (register) after it is sent from the random pattern generation register (PAGR) to the multiple input signature register (MISR). In other words, this compressed data stored in the MISR is not compressed data from a processor. Additionally, Hayashi does not teach that the compressed data in the MISR might be a compressed command. Hayashi merely refers to the compressed data as "data," generally. Therefore, Hayashi does not teach or suggest control logic to decode a compressed command from a processor.

In contrast, claim 12 recites "control logic to decode a compressed command from the processor." For the reasons stated above, White and Hayashi, either alone or in combination, fail to teach or suggest all of the limitations of the claim. In particular, the cited references do not teach or suggest control logic to decode a compressed command from the processor. Therefore, White and Hayashi, either alone or in combination, do not teach or suggest the processor sends a command based self test to the first intelligence wrapper at a first speed and the control logic executes the operations associated with that command at a second speed asynchronous with the first speed.

Given that the cited references fail to teach or suggest all of the limitations of the claim, Applicant respectfully submits that claim 12 is patentable over the cited references. Moreover, the claim is patentable over the cited references because there is the Office Action fails to establish a motivation to combine the references. Accordingly, Applicant requests that the rejection of claim 12 under 35 U.S.C. § 103(a) be withdrawn.

Independent claim 21, as amended, also includes a limitation that is similar to the limitation of claim 12. Given that the claims include similar limitations, even though each claim should be interpreted according to the language of the claim itself and not other claims, claim 21 should be patentable over the cited reference for at least the same reasons as claim 12. Claim 21 also may be patentable over the cited reference for additional reasons. Accordingly, Applicant requests that the rejection of claim 21 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 13-20 and 22-24 depend from independent claims 12 and 21, which are patentable over the cited reference, Applicant respectfully submits that

dependent claims 13-20 and 22-24 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 13-20 and 22-24 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Jeffrey Holman at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,
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